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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIFTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2017

Course Code: EC361

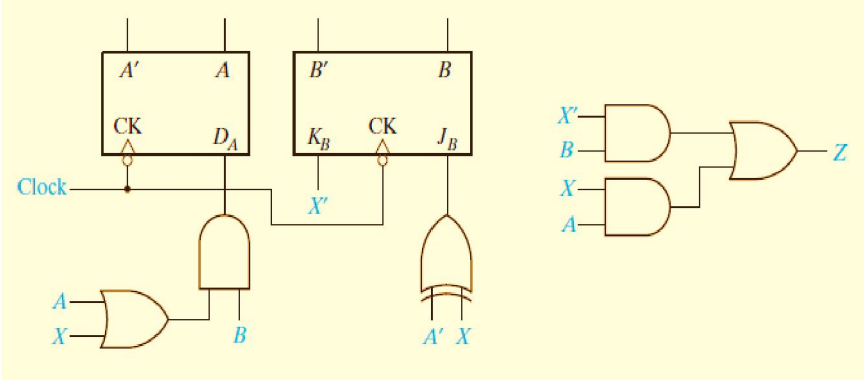
Course Name: DIGITAL SYSTEM DESIGN (EC, AE)

Max. Marks: 100 Duration: 3 Hours

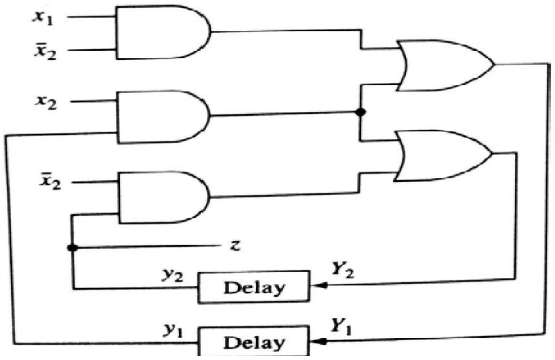
PART A

Answer any two full questions, each carries 15 marks. Marks

1 a) Analyse the following sequential network. Derive the next state and output equations. Obtain its transition table and state table. (7.5)



b) Analyse the asynchronous sequential network shown in figure, by forming the excitation/transition table, state table, flow table, and flow diagram. The network operates in the fundamental mode with the restriction that only one input variable can change at a time. (7.5)



2 a) Draw the ASM chart for a mod 8 binary up-down counter (7.5)

b) One type of clocked T-Flip-flop works as follows: (7.5)
The flip-flop has two inputs, T and P. The flip- flop will change state if T=1 when the clock(P) changes from 1 to 0. Under all other conditions, Q should remain constant. Assume that T and P do not change simultaneously. Obtain a minimal flow table.

3 a) Reduce the following State table using implication chart. (7.5)

Present State	Next State $X=0$	Next State 1	Present Output
a	d	c	0
b	f	h	0
c	e	d	1
d	a	e	0
e	c	a	1
f	f	b	1
g	b	h	0
h	c	g	1

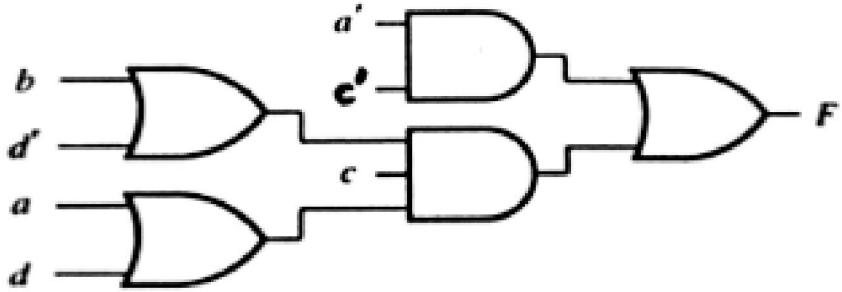
b) The reduced flow table shown below for a fundamental mode asynchronous sequential network. Determine a state assignment involving a minimum number of variables that allows a realization free of critical races. Construct the corresponding transition table and obtain the minimal-sum expressions for realisations using feedback loops. Assume that both the inputs won't change simultaneously (7.5)

Present State	Next state				Output(z)			
	Input State(x_1,x_2)				Input State(x_1,x_2)			
	00	01	10	11	00	01	10	11
1	①	①	4	①	0	0	-	0
2	②	1	3	-	1	-	-	-
3	2	③	③	③	-	1	1	1
4	1	-	④	3	-	-	0	-

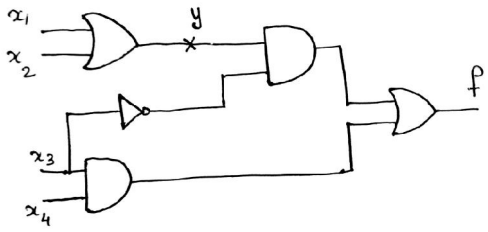
PART B

Answer any two full questions, each carries 15 marks.

4 a) Find all of the static hazards in the following network. For each hazard, specify the values of the variables which are constant and the variable which are changing. Indicate how all of these hazards could be eliminated by adding gates to the existing networks. (7.5)



b) For the given circuit, find the tests to detect the faults x_3 S-A-0, x_3 S-A-1, yS-A-0 and yS-A-1. (7.5)



5 a) Explain Essential hazards in asynchronous sequential networks. What are the constraints to be satisfied to avoid Essential hazards? (7.5)

b) Explain Kohavi algorithm. (7.5)

6 a) Differentiate positive skew and negative skew. (3.5)

b) Explain Jitter. What causes Jitter? (4)

c) Explain different test pattern generation for BIST. (7.5)

PART C

Answer any two full questions, each carries 20 marks.

7 a) Explain different kinds of PLA folding. (10)

	b)	Draw and explain the architecture of Xilinx 9500-family CPLDs. Also explain the function block architecture.	(10)
8	a)	Describe the different test generation techniques for PLA.	(10)
	b)	Explain the internal structure of an XC4000-series CLB.	(10)
9	a)	Explain different testable PLA Designs.	(10)
	b)	Using suitable illustrations explain the XC4000 programmable interconnect.	(10)

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